PATENT APPLICATION
DOCKET NO.: 200207723-1

LISTING OF THE CLAIMS

Pursuant to 37 C.F.R. §1.121, provided below is a listing of the claims.

1. (Original) A controller arrangement for effectuating data transfer between a core clock domain and a bus clock domain, wherein said core clock domain is operable with a core clock signal and said bus clock domain is operable with a bus clock signal, said core and bus clock signals having a ratio, comprising:

a bus clock synchronizer controller portion operating to generate a set of clock relationship control signals, wherein at least a portion of said clock relationship control signals are used in generating a set of bus domain synchronizer control signals towards a bus-to-core synchronizer and a core-to-bus synchronizer; and

a core clock synchronizer controller portion operating to generate a set of core domain synchronizer control signals towards said bus-to-core synchronizer and said core-to-bus synchronizer, said core clock synchronizer controller portion operating responsive to said clock relationship control signals provided by said bus clock synchronizer controller portion and configuration

information indicative of different skew tolerances and latency values associated with at least one of said bus clock and core clock signals.

2. (Original) The controller arrangement as recited in claim 1, wherein said bus clock synchronizer controller portion is operable responsive to a SYNC pulse that is sampled in said bus clock domain by said bus clock signal.

3. (Original) The controller arrangement as recited in claim 2, wherein said SYNC pulse is generated by a phase-locked loop (PLL) when a rising edge in said core clock signal is at least substantially coincident with a rising edge in said bus clock signal.

4. (Original) The controller arrangement as recited in claim 2, wherein said core clock synchronizer controller portion is operable responsive to said SYNC pulse that is sampled in said core clock domain by said core clock signal.

5. (Currently Amended) The controller arrangement as recited in claim 4, wherein said bus clock synchronizer controller portion comprises:

a sync counter and a ratio detector operating responsive to said sampled SYNC pulse in said bus clock domain for determining a sync_ratio signal;

a cycle generator operating responsive to said sync_ratio signal and said sampled SYNC pulse in said bus clock domain for generating a cycle information signal indicative of a current clock cycle;

a sequence generator operating responsive to said sync_ratio signal and said sampled SYNC pulse in said bus clock domain for generating a sequence signal; and

a bus domain synchronizer control signal generator block operating responsive to said sync_ratio signal, said sequence signal and said cycle information signal for generating said set of bus domain synchronizer control signals towards said bus-to-core synchronizer and said core-to-bus synchronizer, wherein said sync_ratio signal and said sequence signal are provided as part of said set of clock relationship control signals to said core clock synchronizer controller portion.

6. (Original) The controller arrangement as recited in claim 5, wherein said core clock synchronizer controller portion comprises a core domain synchronizer control signal generator block operating responsive to said configuration information and a plurality of internal control signals manufactured based on said set of clock relationship control signals provided by said bus clock synchronizer controller portion, for generating said set of core domain synchronizer control signals towards said bus-to-core synchronizer and said core-to-bus synchronizer.

7. (Original) The controller arrangement as recited in claim 6, wherein said core clock synchronizer controller portion is further operable to generate a set of transfer control signals indicative of when valid data transfer can occur between said bus clock domain's circuitry and said core clock domain's circuitry.

8. (Original) The controller arrangement as recited in claim 6, wherein said core clock synchronizer controller portion further comprises a skew state detector for generating a skew_state control signal indicative of a current skew relationship between said bus clock and core clock signals, said skew_state control signal being provided to said core domain synchronizer control signal generator block for generating said set of core domain synchronizer control signals towards said bus-to-core synchronizer and said core-to-bus synchronizer.

9. (Original) The controller arrangement as recited in claim 6, wherein said bus clock synchronizer controller portion further comprises a sync delay block operating responsive to said sync_ratio signal and said sampled SYNC pulse in said bus clock domain for generating a syncb0 signal, said syncb0 signal being provided as part of said set of clock relationship control signals to said core clock synchronizer controller portion.

10. (Original) A controller arrangement operable with a programmable synchronizer system for effectuating data transfer between core logic circuitry disposed in a core clock domain and bus logic circuitry disposed in a bus clock domain, wherein said core clock domain is operable with a core clock signal and said bus clock domain is operable with a bus clock signal, said core and bus clock signals having a ratio of N core clock cycles to M bus clock cycles, where $N/M \geq 1$, comprising:

means disposed in said bus clock domain for generating a set of clock relationship control signals responsive to a SYNC pulse that is sampled in said bus clock domain, wherein at least a portion of said clock relationship control signals are used in generating a set of bus domain synchronizer control signals towards a bus-to-core synchronizer and a core-to-bus synchronizer; and

means disposed in said core clock domain for generating a set of core domain synchronizer control signals towards said bus-to-core synchronizer and said core-to-bus synchronizer, said means disposed in said core clock domain operating responsive to said SYNC pulse that is sampled in said core clock domain and to said clock relationship control signals provided by said means disposed in said bus clock domain, wherein a configuration interface provides configuration information to said means disposed in said

core clock domain for compensating for at least one of a variable skew factor and a variable latency factor associated with said core clock signal.

11. (Currently Amended) The controller arrangement ~~operable with a programmable synchronizer system~~ as recited in claim 10, wherein said means disposed in said bus clock domain comprises:

a sync counter and a ratio detector operating responsive to said sampled SYNC pulse in said bus clock domain for determining a sync_ratio signal;

a cycle generator operating responsive to said sync_ratio signal and said sampled SYNC pulse in said bus clock domain for generating a cycle information signal indicative of a current clock cycle;

a sequence generator operating responsive to said sync_ratio signal and said sampled SYNC pulse in said bus clock domain for generating a sequence signal; and

a bus domain synchronizer control signal generator block operating responsive to said sync_ratio signal, said sequence signal and said cycle information signal for generating said set of bus domain synchronizer control signals towards said bus-to-core

synchronizer and said core-to-bus synchronizer, wherein said sync_ratio signal and said sequence signal are provided as part of said set of clock relationship control signals to said means disposed in said core clock domain.

12. (Currently Amended) The controller arrangement ~~operable with a programmable synchronizer system~~ as recited in claim 11, wherein said means disposed in said core clock domain comprises a core domain synchronizer control signal generator block operating responsive to said configuration information and a plurality of internal control signals manufactured based on said set of clock relationship control signals provided by said means disposed in said bus clock domain, for generating said set of core domain synchronizer control signals towards said bus-to-core synchronizer and said core-to-bus synchronizer and for generating a set of transfer control signals indicative of when valid data transfer can occur between said bus logic circuitry and said core logic circuitry.

13. (Currently Amended) The controller arrangement ~~operable with a programmable synchronizer system~~ as recited in claim 12, wherein said SYNC pulse is generated by a phase-locked loop (PLL) when a rising edge in said core clock signal is at least substantially coincident with a rising edge in said bus clock signal.

14. (Currently Amended) The controller arrangement ~~operable with a programmable synchronizer system~~ as recited in claim 12, wherein said core-to-bus synchronizer comprises:

a first TRANSMIT multiplex-register (MUXREG) block disposed in said core clock domain, said first TRANSMIT MUXREG block operating to transmit a portion of data responsive to a c0_sel control signal that is registered using said core clock signal, wherein said data is generated in said core clock domain by said core logic circuitry and said c0_sel control signal generated by said core domain synchronizer control signal generator block;

a second TRANSMIT MUXREG block in said core clock domain for transmitting another portion of said data generated in said core clock domain responsive to a c1_sel control signal that is registered using said core clock signal, wherein said c1_sel

control signal is generated by said core domain synchronizer control signal generator block; and

a RECEIVE MUXREG block disposed in said bus clock domain for receiving said data from said first and second TRANSMIT MUXREG blocks in a serial fashion responsive to a bus_sel control signal that is registered using said bus clock signal, wherein said bus_sel control is generated by said bus domain synchronizer control signal generator block.

15. (Currently Amended) The controller arrangement ~~operable with a programmable synchronizer system~~ as recited in claim 14, wherein said core logic circuitry is operable responsive to a c2b_valid signal provided as part of said transfer control signals by said core domain synchronizer control signal generator block.

16. (Currently Amended) The controller arrangement ~~operable with a programmable synchronizer system~~ as recited in claim 15, wherein said c2b_valid signal, said c0_sel control signal and said c1_sel control signal are programmable for different skew tolerance and latency values based on said configuration information.

17. (Currently Amended) The controller arrangement ~~operable with a programmable synchronizer system~~ as recited in claim 12, wherein said means disposed in said core clock domain further comprises a skew state detector for generating a skew_state control signal indicative of a current skew relationship between said bus clock and core clock signals, said skew_state control signal being provided to said core domain synchronizer control signal generator block.

18. (Currently Amended) The controller arrangement ~~operable with a programmable synchronizer system~~ as recited in claim 12, wherein said means disposed in said bus clock domain further comprises a sync delay block operating responsive to said sync_ratio signal and said sampled SYNC pulse in said bus clock domain for generating a syncb0 signal, said syncb0 signal being provided as part of said set of clock relationship control signals to said means disposed in said core clock domain.

19. (Currently Amended) The controller arrangement ~~operable with a programmable synchronizer system~~ as recited in claim 12, wherein said bus-to-core synchronizer comprises:

a first TRANSMIT multiplex-register (MUXREG) block disposed in said bus clock domain, said first TRANSMIT MUXREG block operating to transmit a portion of data responsive to a b0_sel control signal that is registered using said bus clock signal, wherein said data is generated in said bus clock domain by said bus logic circuitry and said b0_sel control signal is generated by said bus domain synchronizer control signal generator block;

a second TRANSMIT MUXREG block in said bus clock domain for transmitting another portion of said data generated in said bus clock domain responsive to a b1_sel control signal that is registered using said bus clock signal, wherein said b1_sel control signal is generated by said bus domain synchronizer control signal generator block; and

a RECEIVE MUXREG block disposed in said core clock domain for receiving said data from said first and second TRANSMIT MUXREG blocks in a serial fashion responsive to a core_sel control signal that is registered using said core clock signal, wherein said core_sel control is generated by said core domain synchronizer control signal generator block.

20. (Currently Amended) The controller arrangement ~~operable with a programmable synchronizer system~~ as recited in claim 19, wherein said core logic circuitry is operable responsive to a b2c_valid signal provided as part of said transfer control signals by said core domain synchronizer control signal generator block.

21. (Currently Amended) The controller arrangement ~~operable with a programmable synchronizer system~~ as recited in claim 20, wherein said b2c_valid signal and said core_sel control signal are programmable for different skew tolerance and latency values based on said configuration information.

22. (Original) A computer system having a controller arrangement operable with a programmable synchronizer apparatus for effectuating data transfer between core logic circuitry disposed in a core clock domain and bus logic circuitry disposed in a bus clock domain, wherein said core clock domain is operable with a core clock signal and said bus clock domain is operable with a bus clock signal, said core and bus clock signals having a ratio of N core clock cycles to M bus clock cycles, where $N/M \geq 1$, comprising:

a bus clock synchronizer controller portion operating to generate a set of clock relationship control signals, wherein at least a portion of said clock relationship control signals are used in generating a set of bus domain synchronizer control signals towards a bus-to-core synchronizer and a core-to-bus synchronizer; and

a core clock synchronizer controller portion operating to generate a set of core domain synchronizer control signals towards said bus-to-core synchronizer and said core-to-bus synchronizer, said core clock synchronizer controller portion operating responsive to said clock relationship control signals provided by said bus clock synchronizer controller portion and configuration information indicative of different skew tolerances and latency

values associated with at least one of said bus clock and core clock signals.

23. (Original) The computer system as recited in claim 22, wherein said bus clock synchronizer controller portion is operable responsive to a SYNC pulse that is sampled in said bus clock domain by said bus clock signal.

24. (Original) The computer system as recited in claim 23, wherein said SYNC pulse is generated by a phase-locked loop (PLL) when a rising edge in said core clock signal is at least substantially coincident with a rising edge in said bus clock signal.

25. (Original) The computer system as recited in claim 23, wherein said core clock synchronizer controller portion is operable responsive to said SYNC pulse that is sampled in said core clock domain by said core clock signal.

26. (Currently Amended) The computer system as recited in claim 25, wherein said bus clock synchronizer controller portion comprises:

a sync counter and a ratio detector operating responsive to said sampled SYNC pulse in said bus clock domain for determining a sync_ratio signal;

a cycle generator operating responsive to said sync_ratio signal and said sampled SYNC pulse in said bus clock domain for generating a cycle information signal indicative of a current clock cycle;

a sequence generator operating responsive to said sync_ratio signal and said sampled SYNC pulse in said bus clock domain for generating a sequence signal; and

a bus domain synchronizer control signal generator block operating responsive to said sync_ratio signal, said sequence signal and said cycle information signal for generating said set of bus domain synchronizer control signals towards said bus-to-core synchronizer and said core-to-bus synchronizer, wherein said sync_ratio signal and said sequence signal are provided as part of said set of clock relationship control signals to said core clock synchronizer controller portion.

27. (Original) The computer system as recited in claim 26, wherein said core clock synchronizer controller portion comprises a core domain synchronizer control signal generator block operating responsive to said configuration information and a plurality of internal control signals manufactured based on said set of clock relationship control signals provided by said bus clock synchronizer controller portion, for generating said set of core domain synchronizer control signals towards said bus-to-core synchronizer and said core-to-bus synchronizer.

28. (Original) The computer system as recited in claim 27, wherein said core clock synchronizer controller portion is further operable to generate a set of transfer control signals indicative of when valid data transfer can occur between said bus clock domain's circuitry and said core clock domain's circuitry.

29. (Original) The computer system as recited in claim 27, wherein said core clock synchronizer controller portion further comprises a skew state detector for generating a skew_state control signal indicative of a current skew relationship between said bus clock and core clock signals, said skew_state control signal being provided to said core domain synchronizer control signal generator block for generating said set of core domain synchronizer control signals towards said bus-to-core synchronizer and said core-to-bus synchronizer.

30. (Original) The computer system as recited in claim 27, wherein said bus clock synchronizer controller portion further comprises a sync delay block operating responsive to said sync_ratio signal and said sampled SYNC pulse in said bus clock domain for generating a syncb0 signal, said syncb0 signal being provided as part of said set of clock relationship control signals to said core clock synchronizer controller portion.